Silicon Nano-Transistors and Breaking the 10nm Physical Gate Length Barrier

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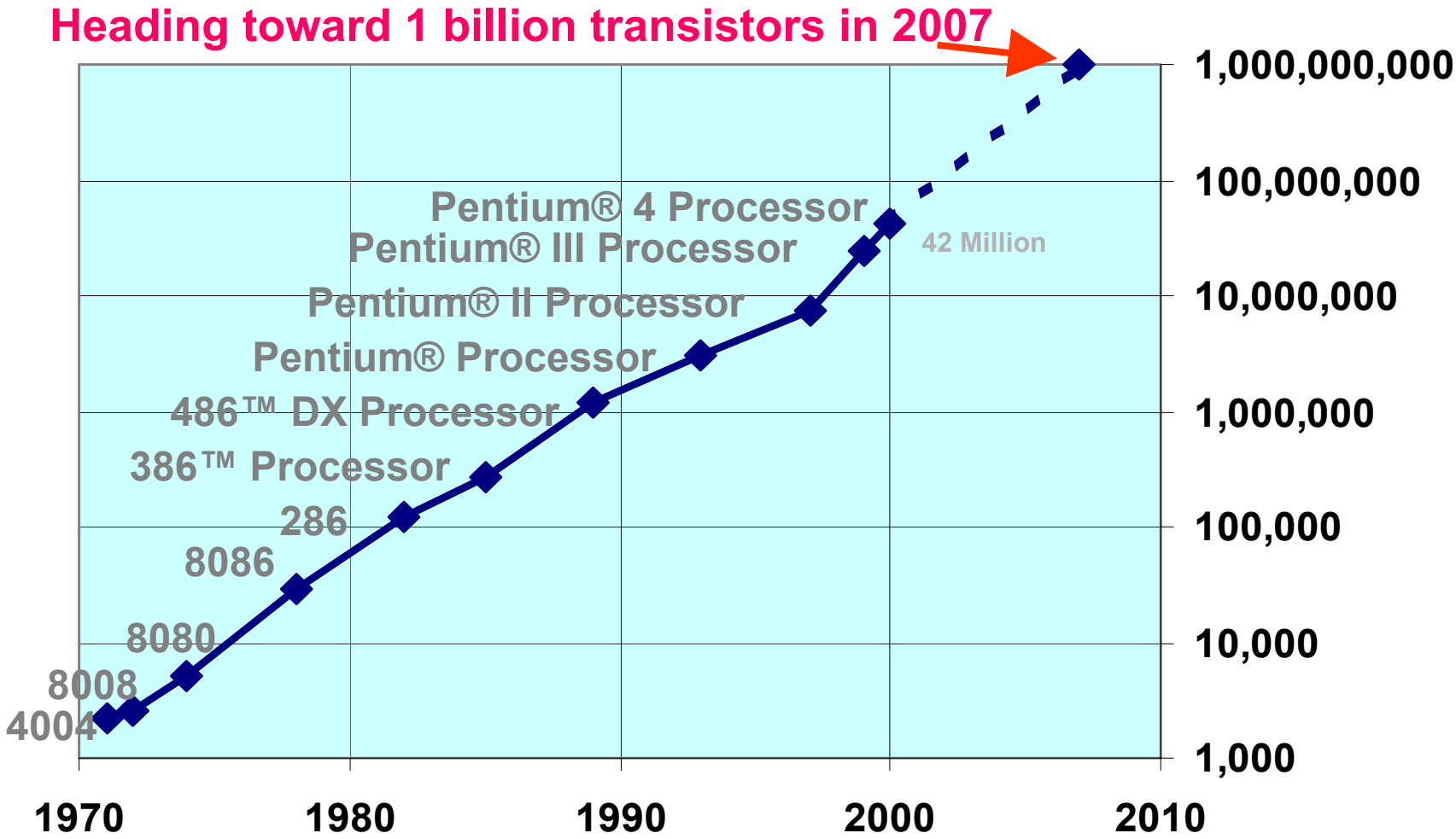
Content

- Introduction
- Device Scaling trends and the 10nm L_G barrier
- New Device Structures
- Gate Dielectric Scaling
- Summary

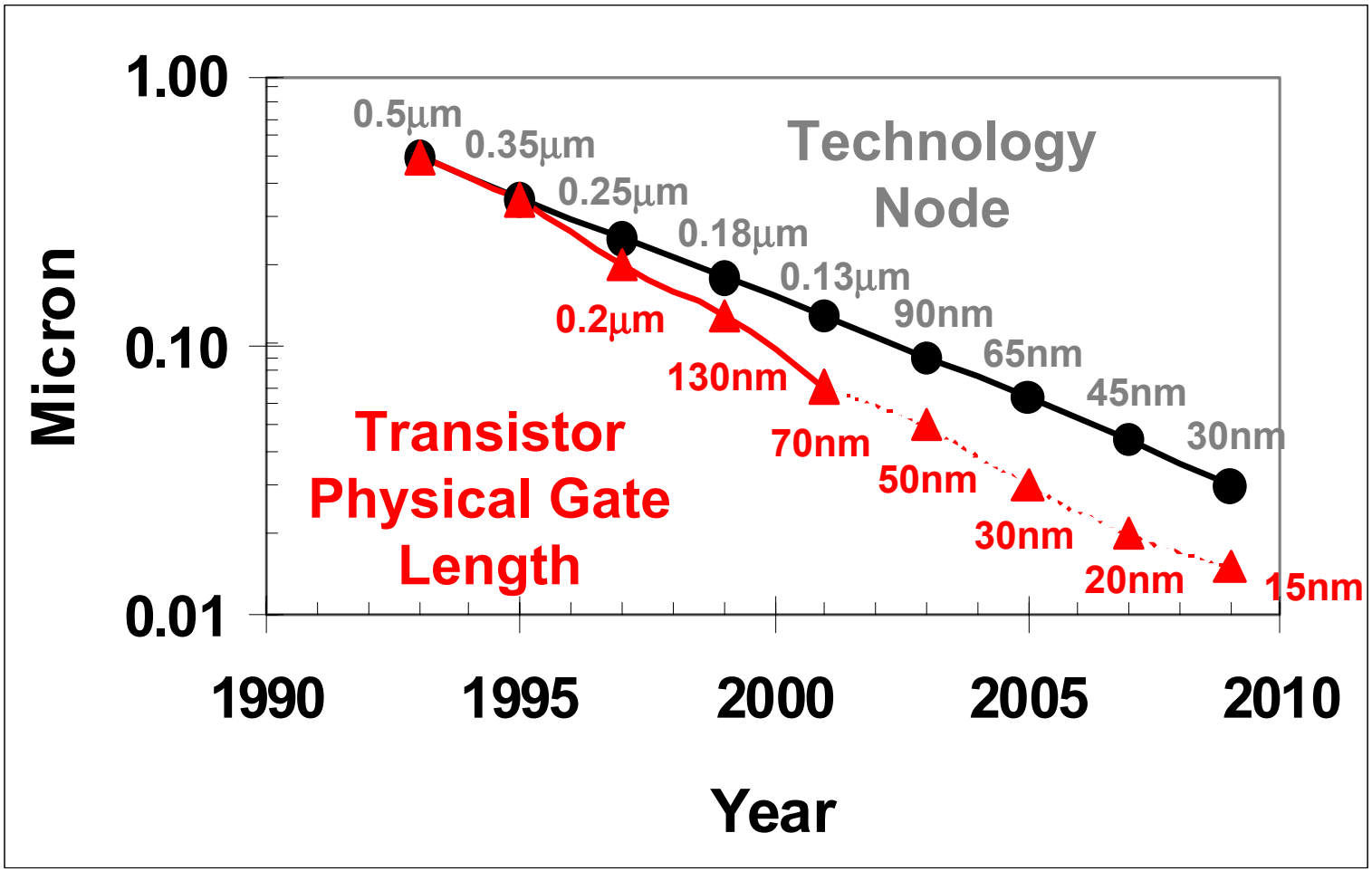
Moore's Law Continues…

– Transistor # doubling every 2 years toward the 1 billion transistor microprocessor



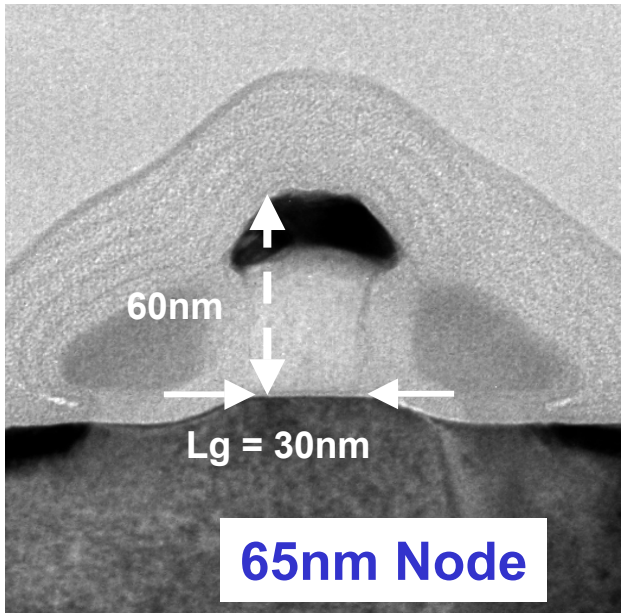
>220M transistors integrated into devices produced today

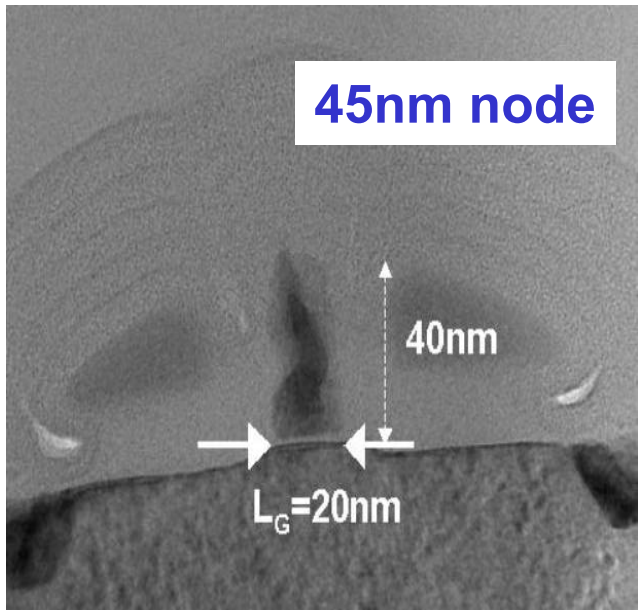
Transistor Physical Gate Length Requirement

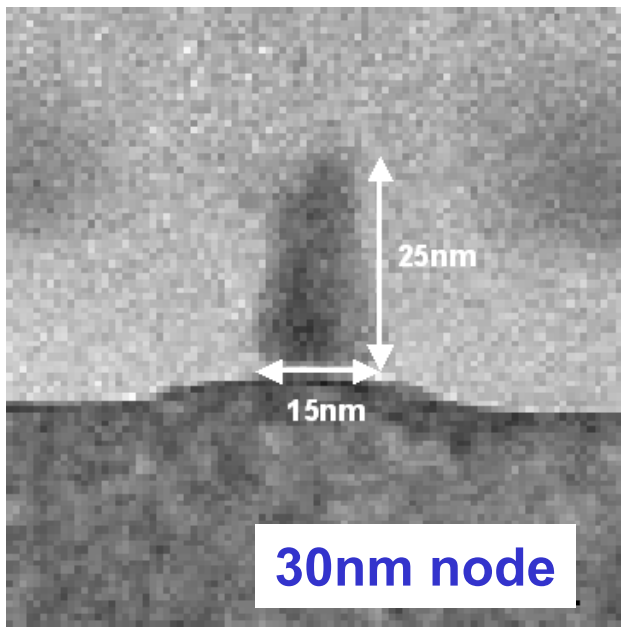


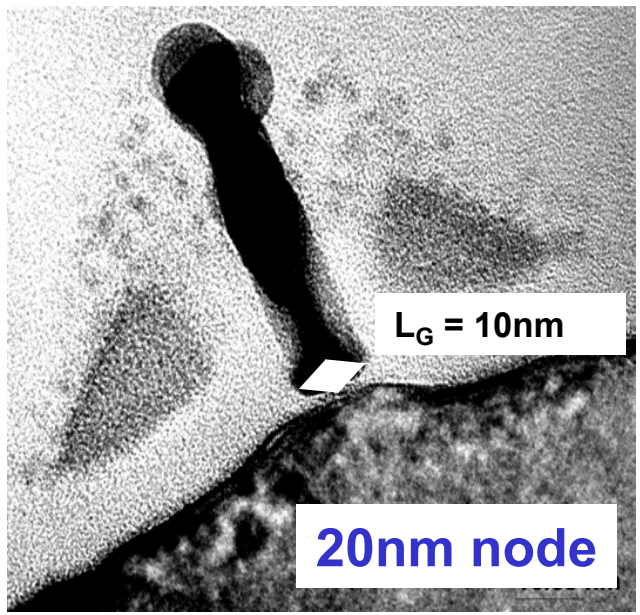
Transistor physical gate length will reach ~15nm before end of this decade, and ~10nm early next decade

Conventional Si Transistor Scaling









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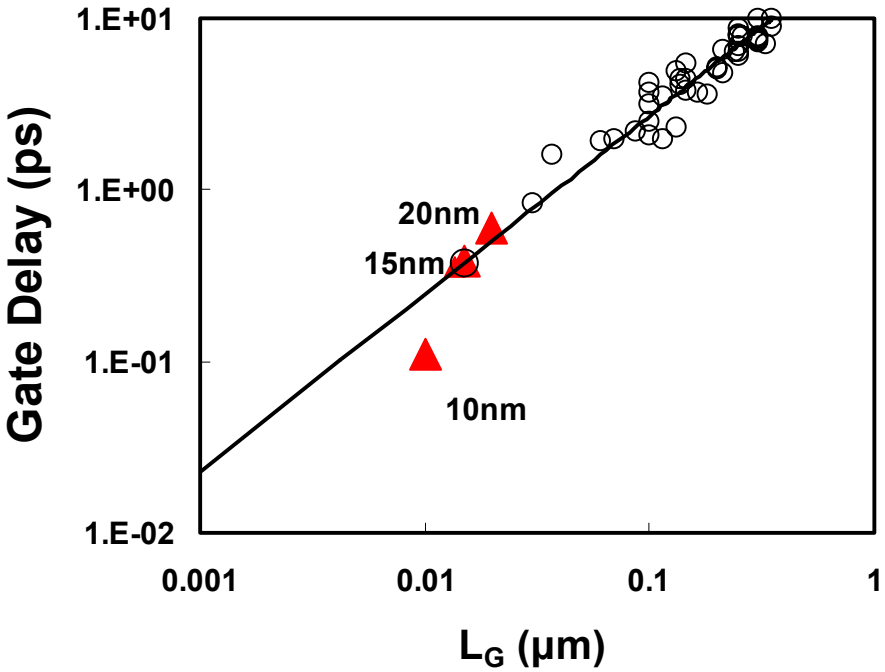
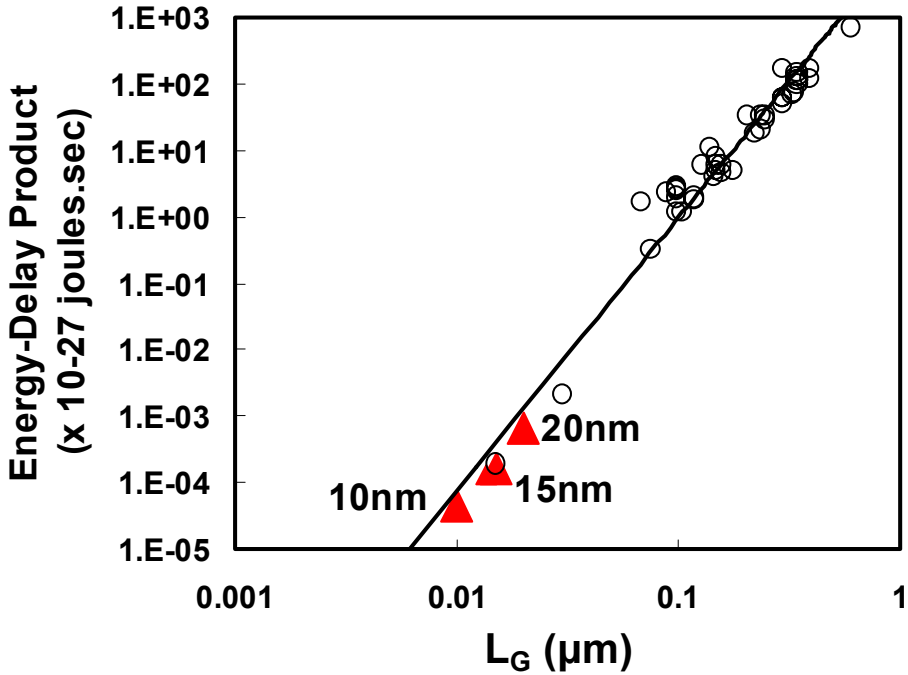
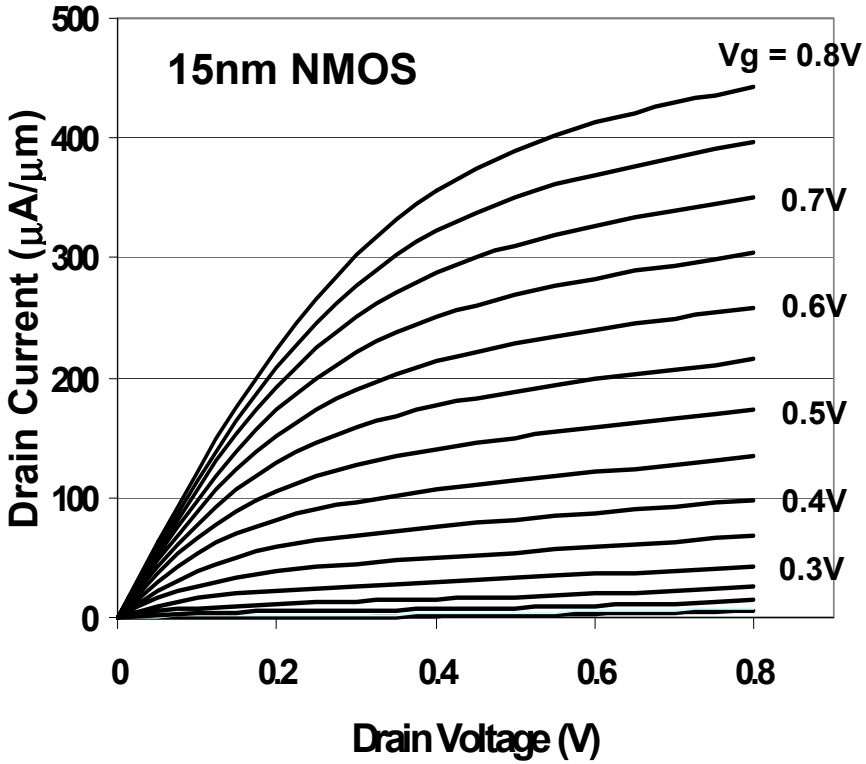
Gate Delay and Energy-Delay Trends

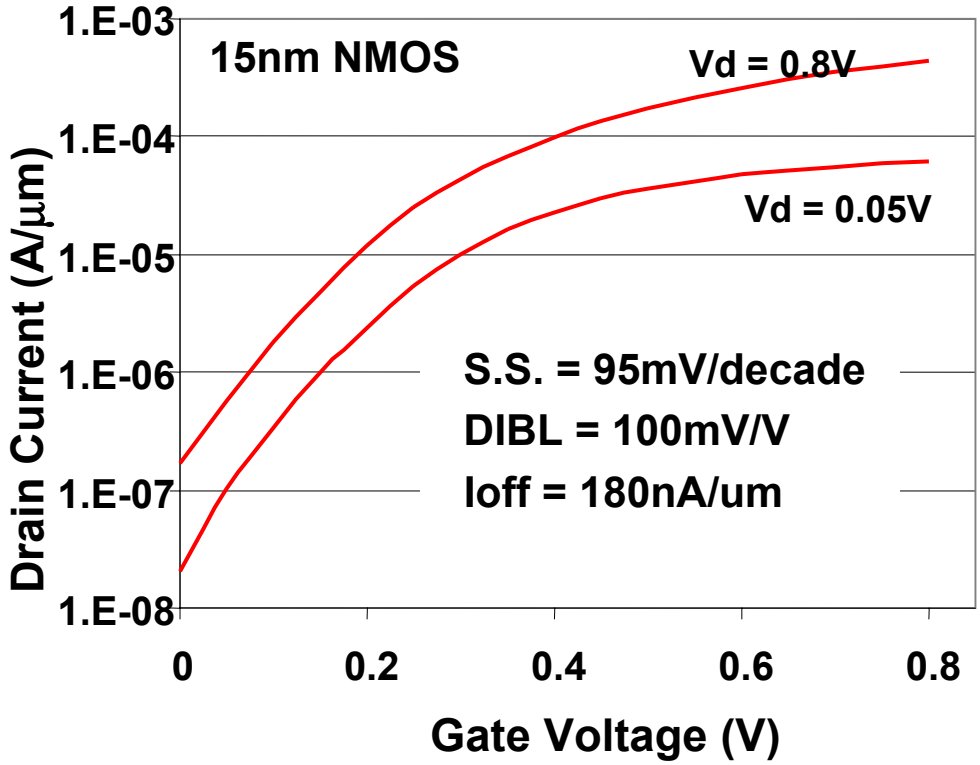




Data from 20nm, 15nm and 10nm research transistors follow the projected trends

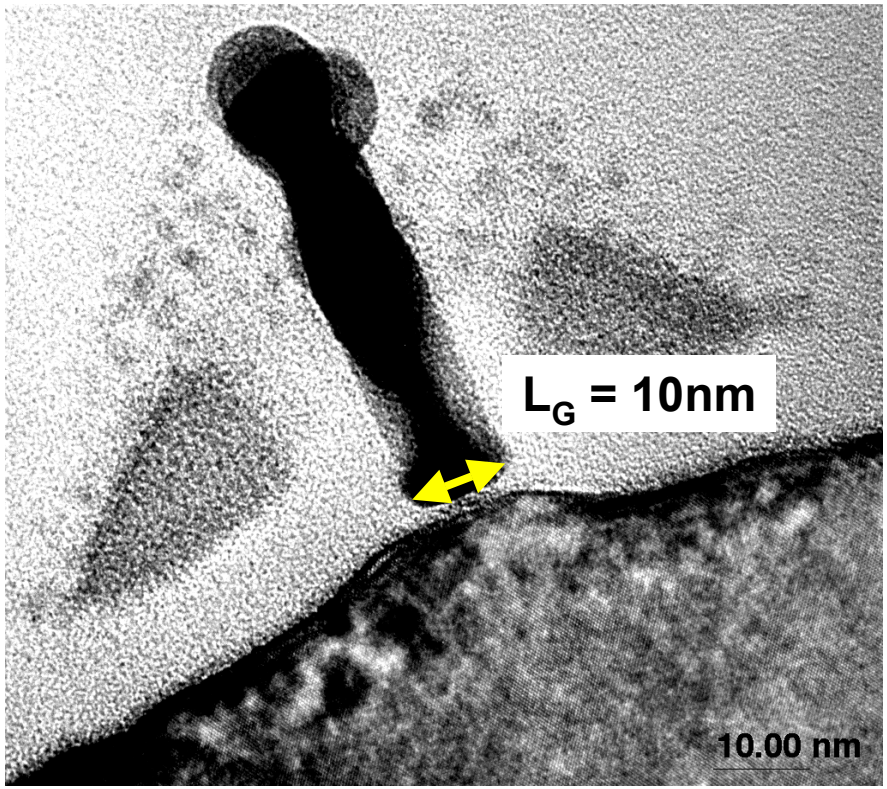
Experimental 15nm Si Nano-Transistor

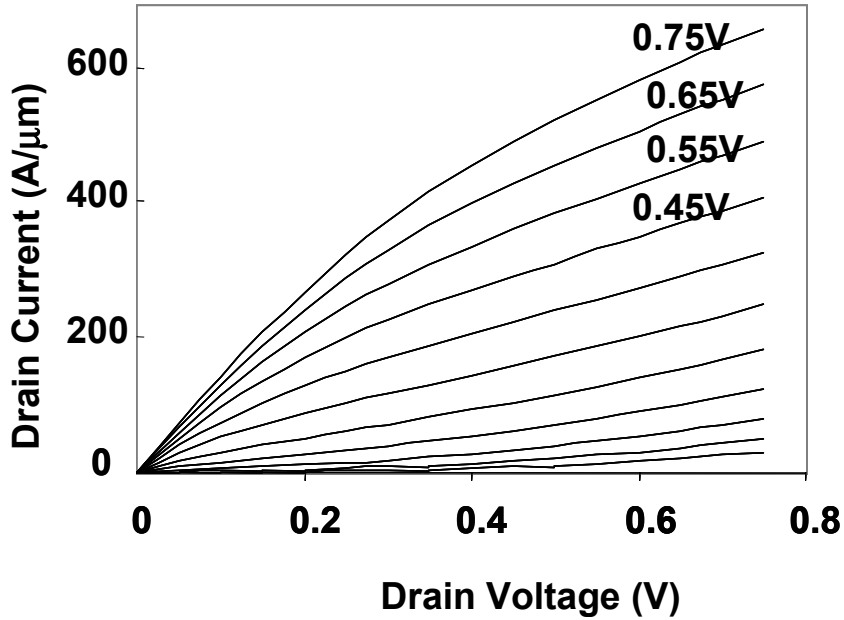


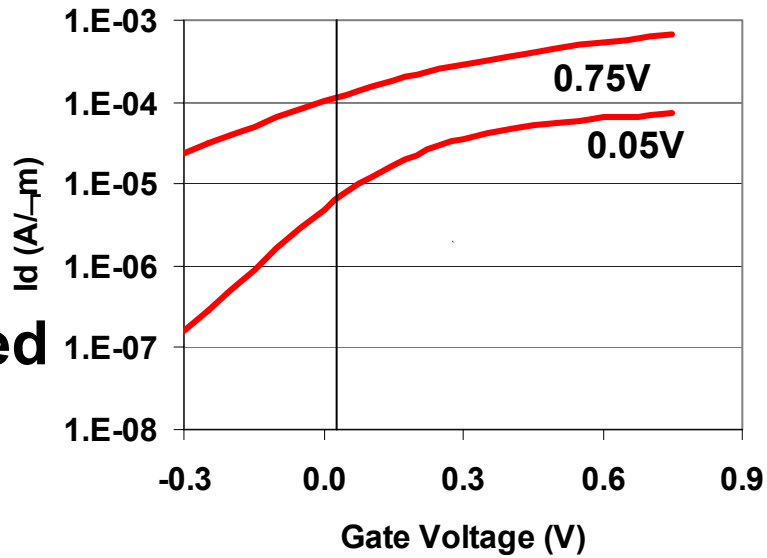


- Electrostatics of 15nm transistor remains intact
- Idsat performance can be further improved using thinner Toxe and various enhancement techniques

Experimental 10nm MOS Transistor

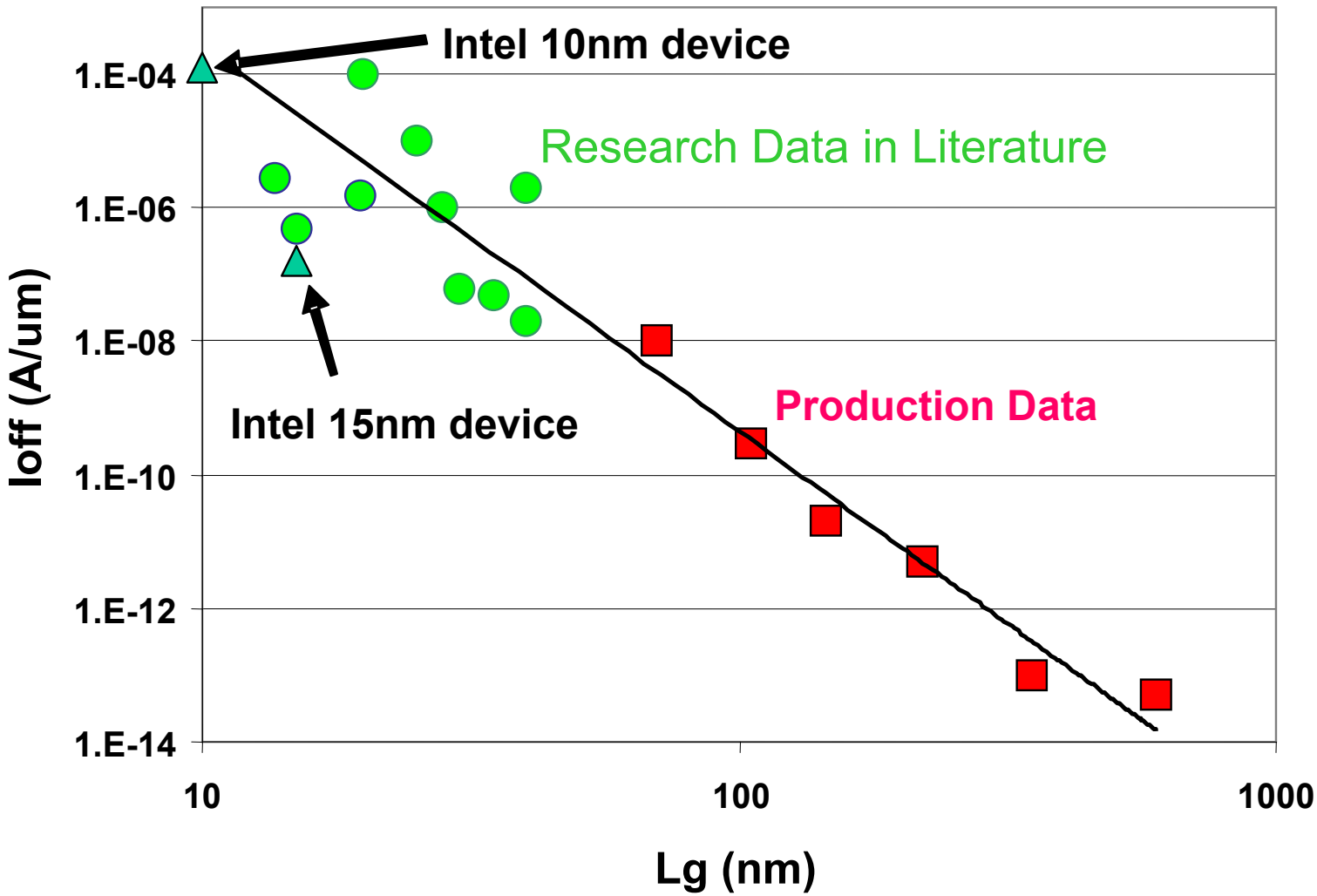




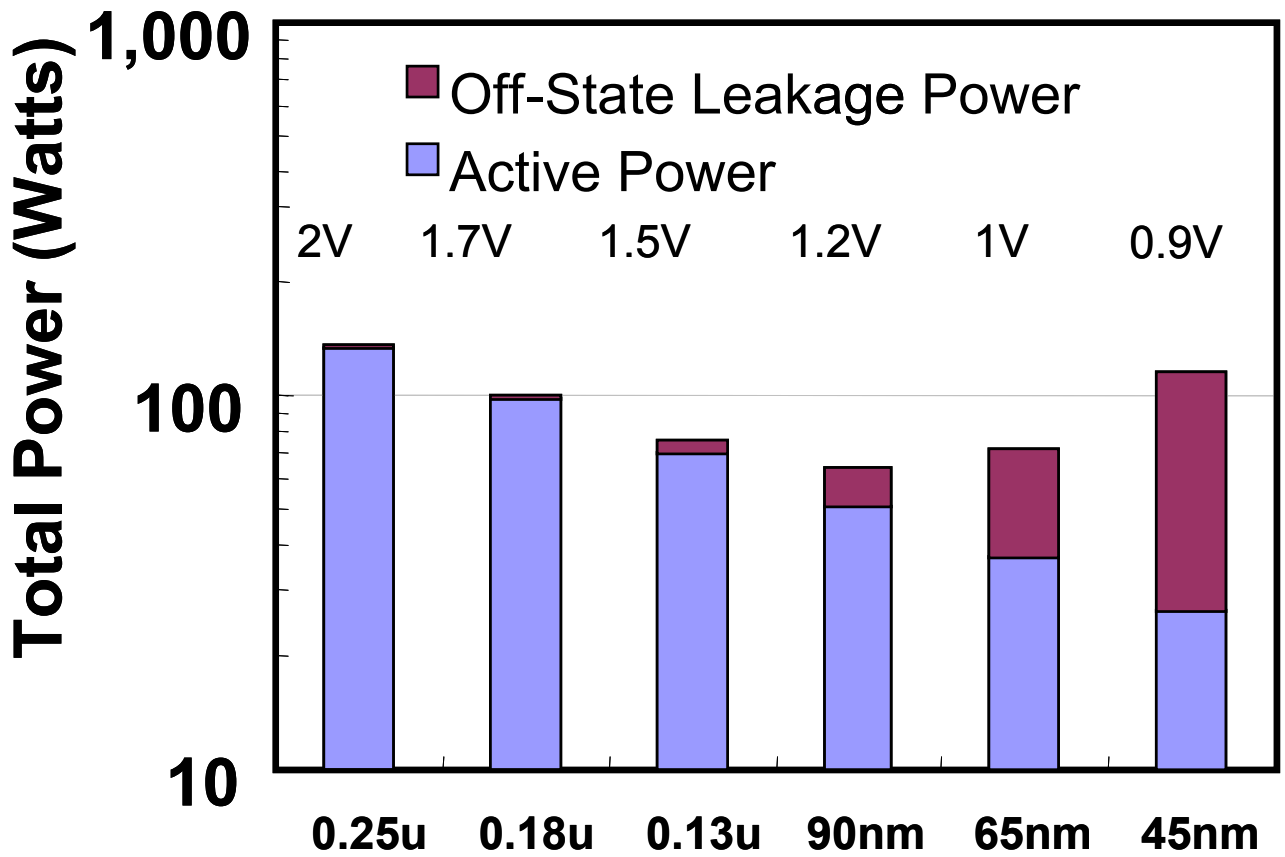


- 10nm transistor shows degraded short channel performance
  - high I_{off}

Transistor Off-state Leakage Trend



Leakage Power is becoming a Larger % of Total Chip Power



Reference: V. De and S. Borkar, "Technology and Design Challenges for Low Power and High Performance," *1999 ISLPED*, pp. 163-168, August 1999.

Potential Solutions to Transistor I_{off} Problem

- Low-temperature operation
- Improve short-channel performance (subthreshold slope & DIBL) using novel device structures
  - Fully-Depleted Transistors
    - Single-gate planar fully depleted SOI
    - Double-gate FINFET
    - Tri-gate

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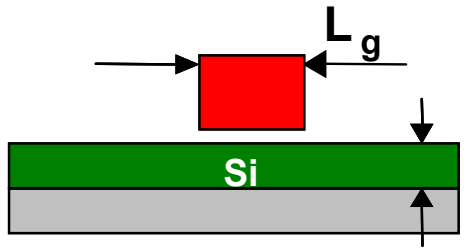
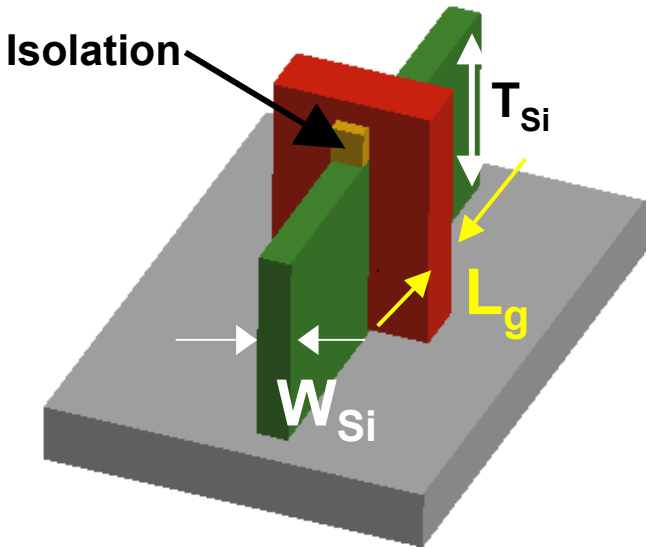
Fully Depleted Transistors



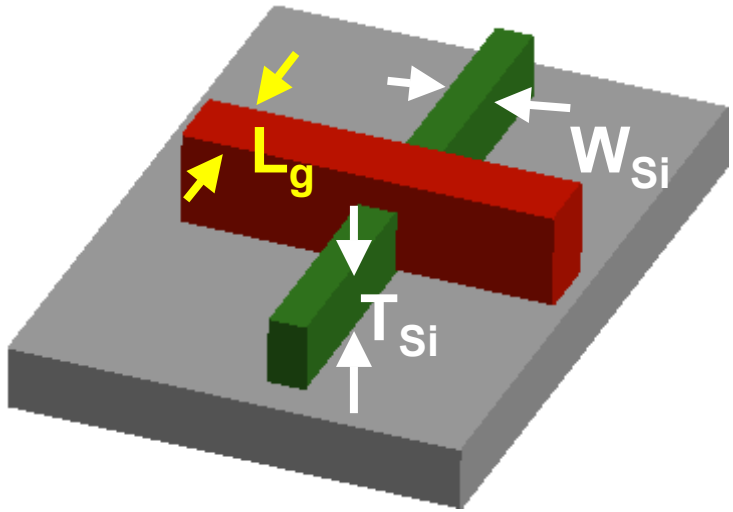
(Planar)

Planar fully depleted SOI



Double-gate (e.g. FINFET)

(Non-Planar)

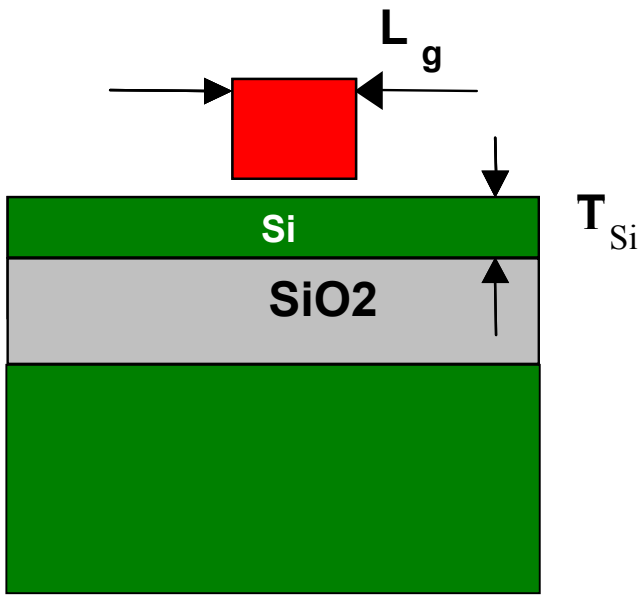


Tri-gate

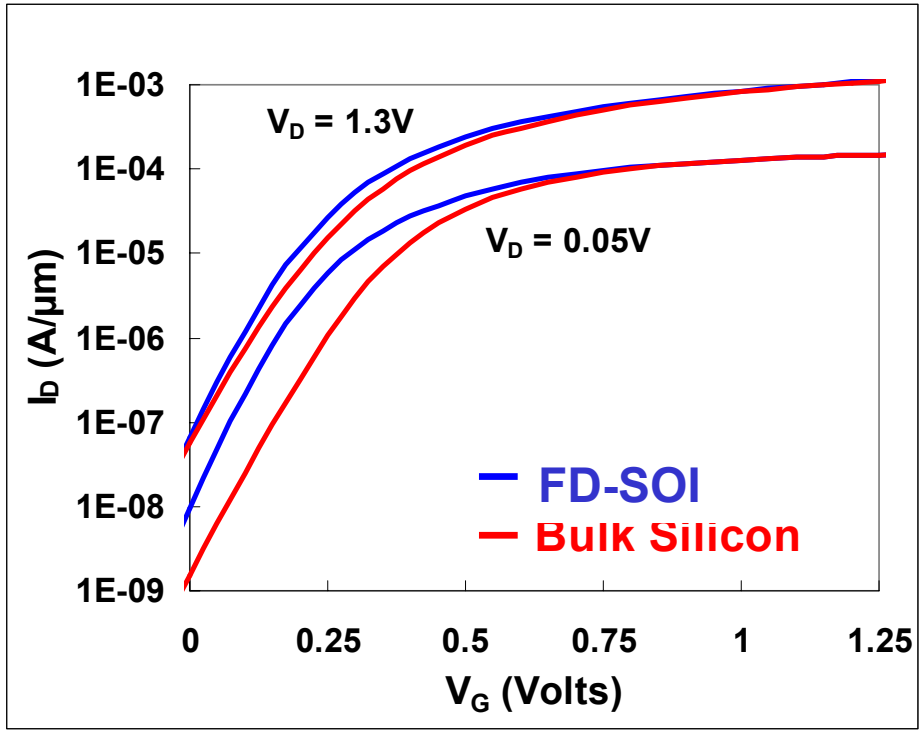
(Non-Planar)

- Fully depleted transistors provide better short channel performance (steeper subthreshold slope and smaller DIBL)

Planar Fully Depleted Transistors

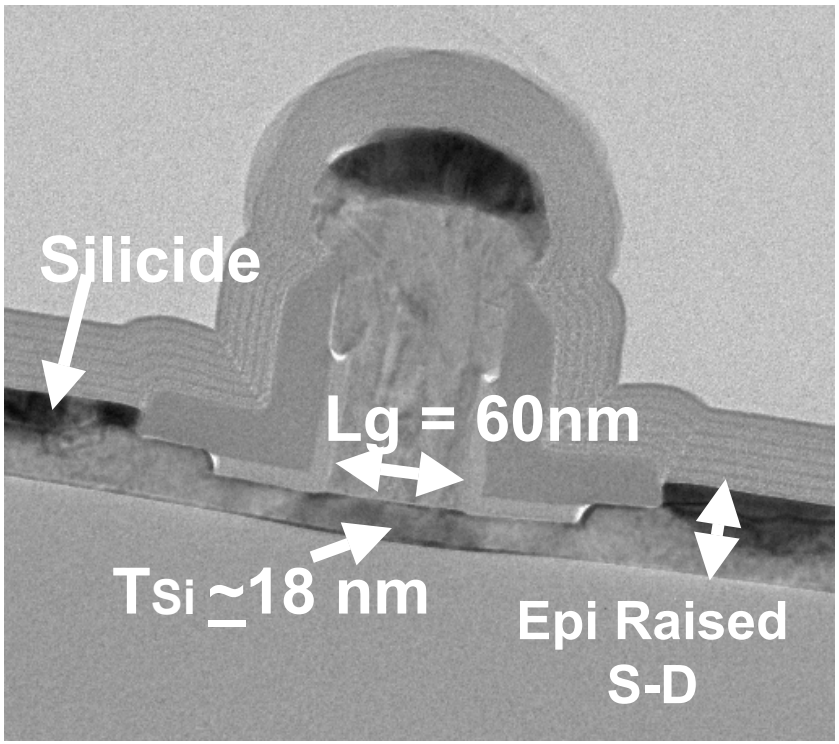


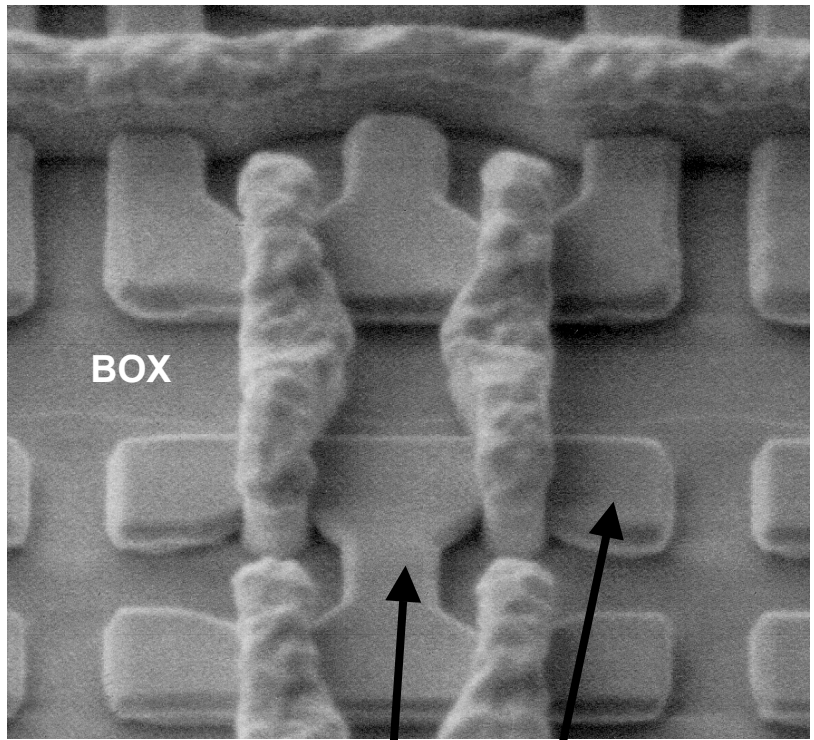
Planar Fully Depleted SOI



- Fully depleted SOI provides steeper subthreshold slope and better DIBL, which can be used to reduce Ioff or increase Idsat
- Cost and controllability of thin Si (T_{Si}) layer are key manufacturing problems

Planar Fully-depleted SOI

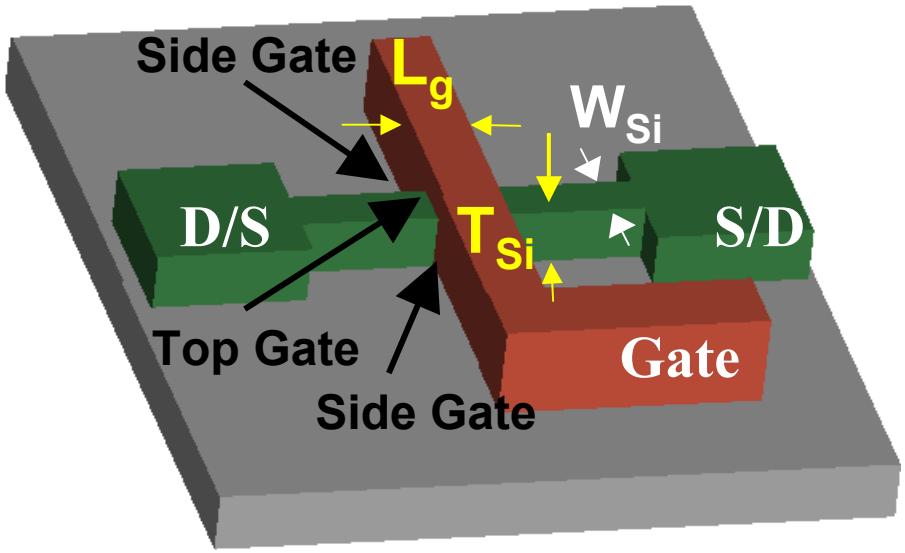


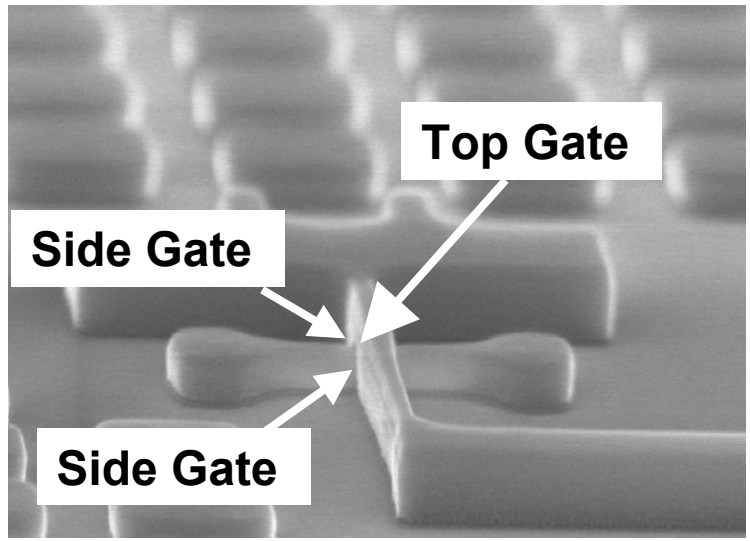


$T_{Si} \leq Lg/3$

Raised S-D using Selective Epi-Si Deposition

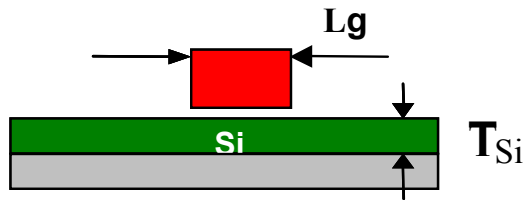
Tri-gate Transistor

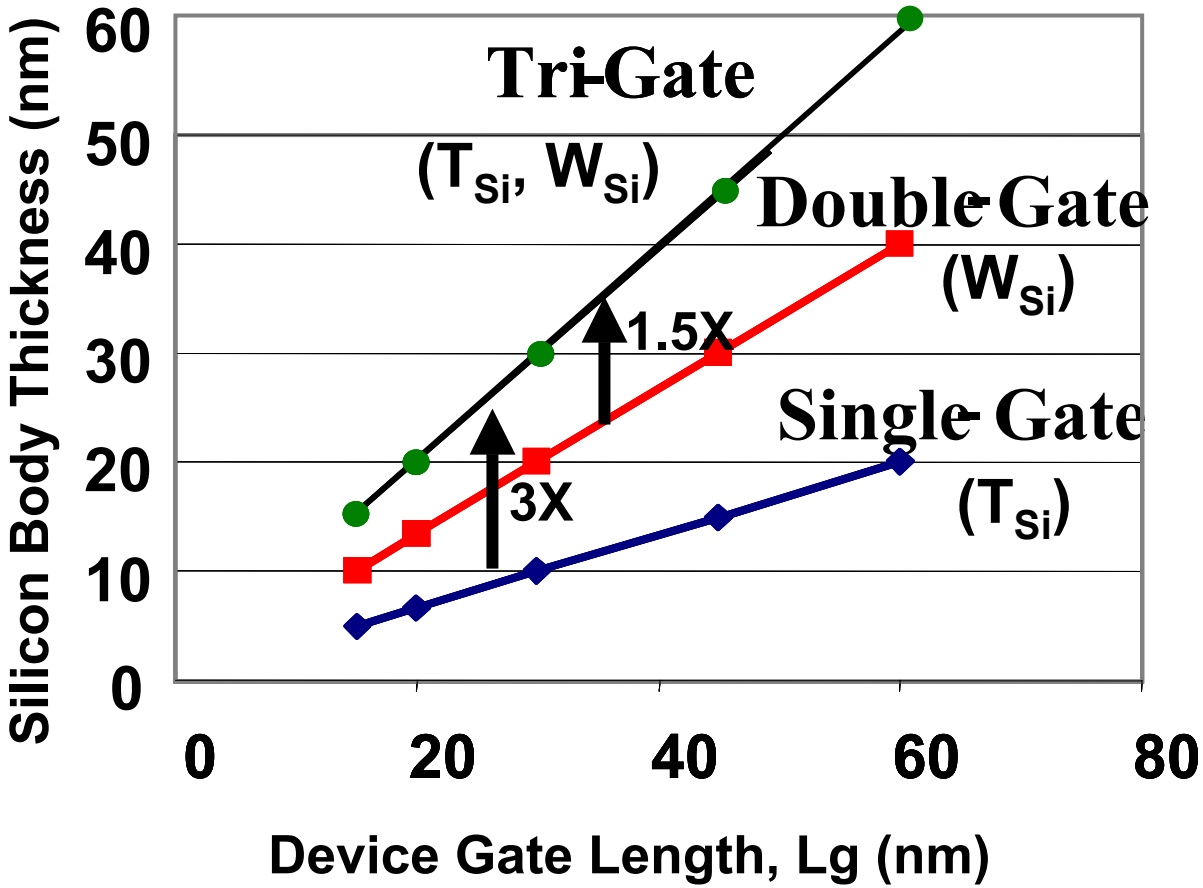


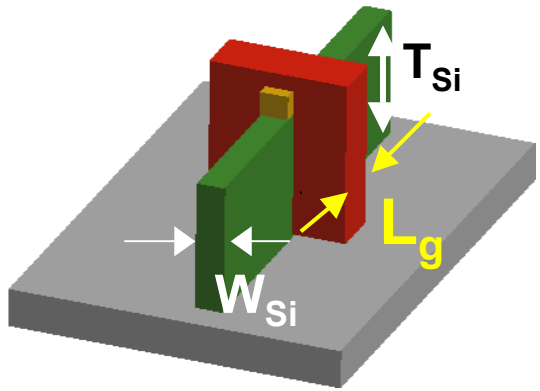


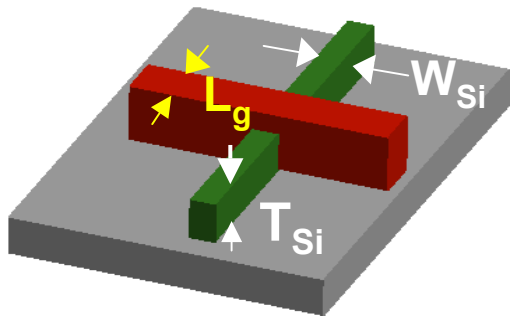
Body controlled on three sides by adjacent Gates: Excellent electrostatic control of body

Tri-gate has the Least Stringent Thickness & Width Requirements

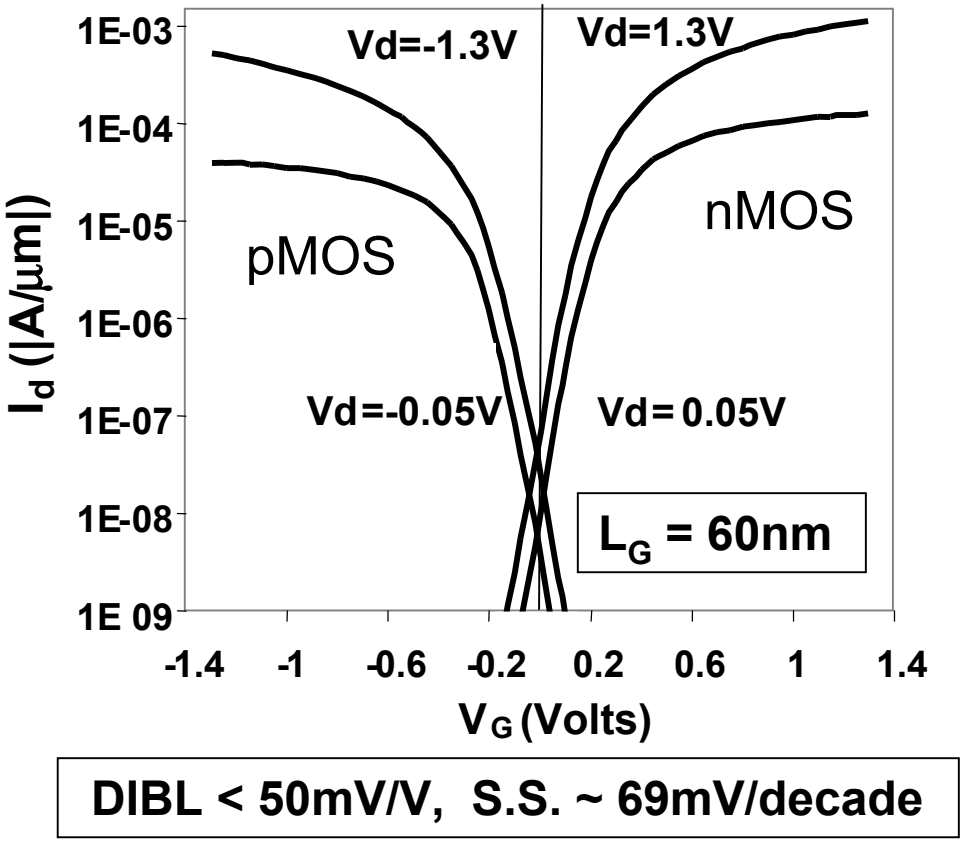




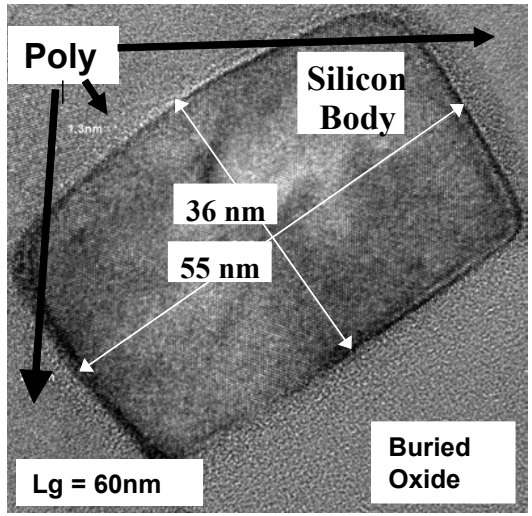


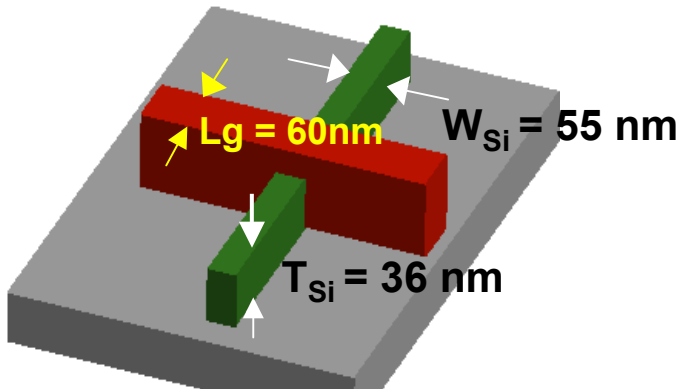


Non-Planar Tri-Gate CMOS Transistor



DIBL < 50mV/V, S.S. ~ 69mV/decade



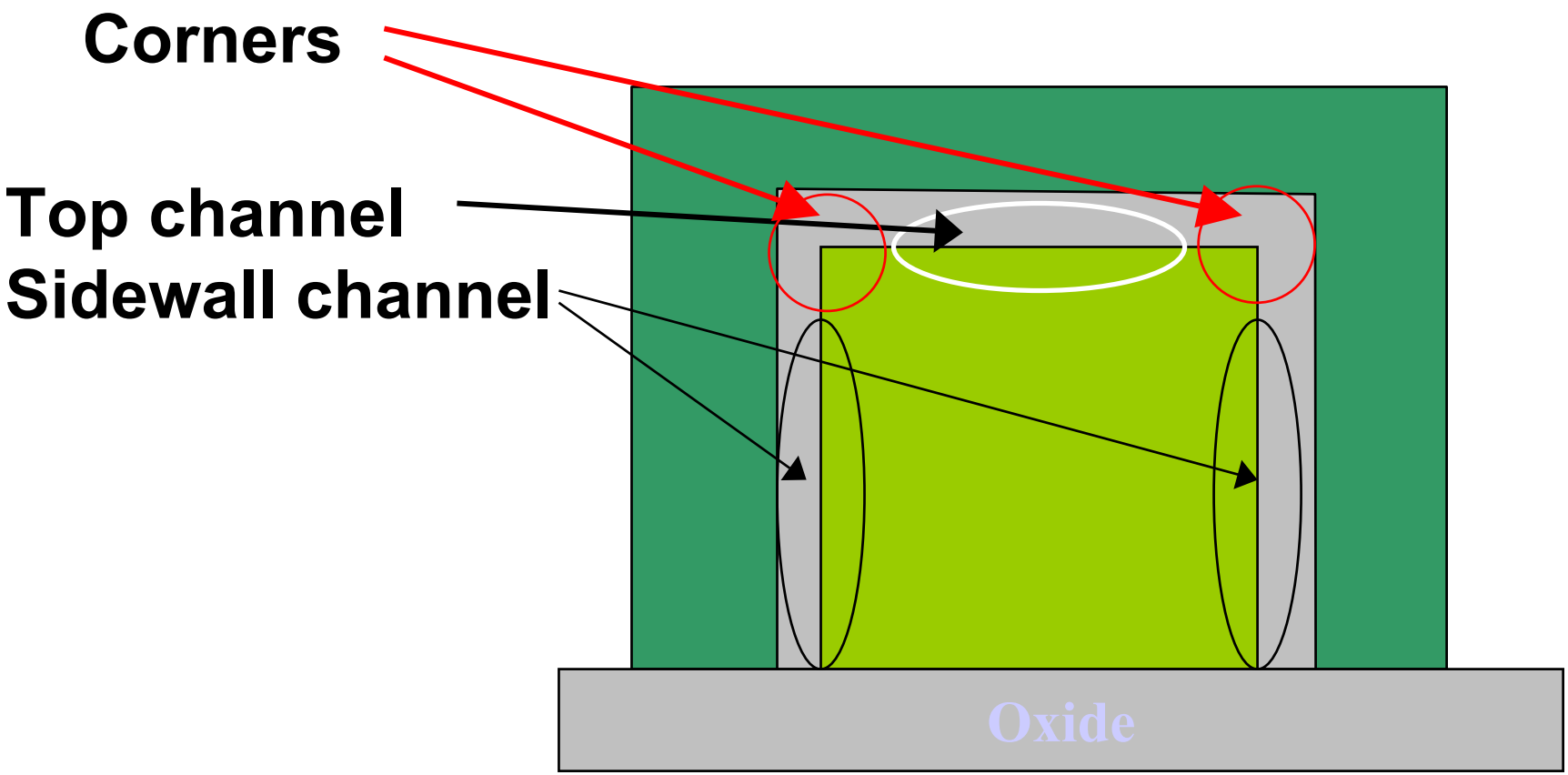


Current per unit width = $I_d/(2*T_{Si}+W_{Si})$

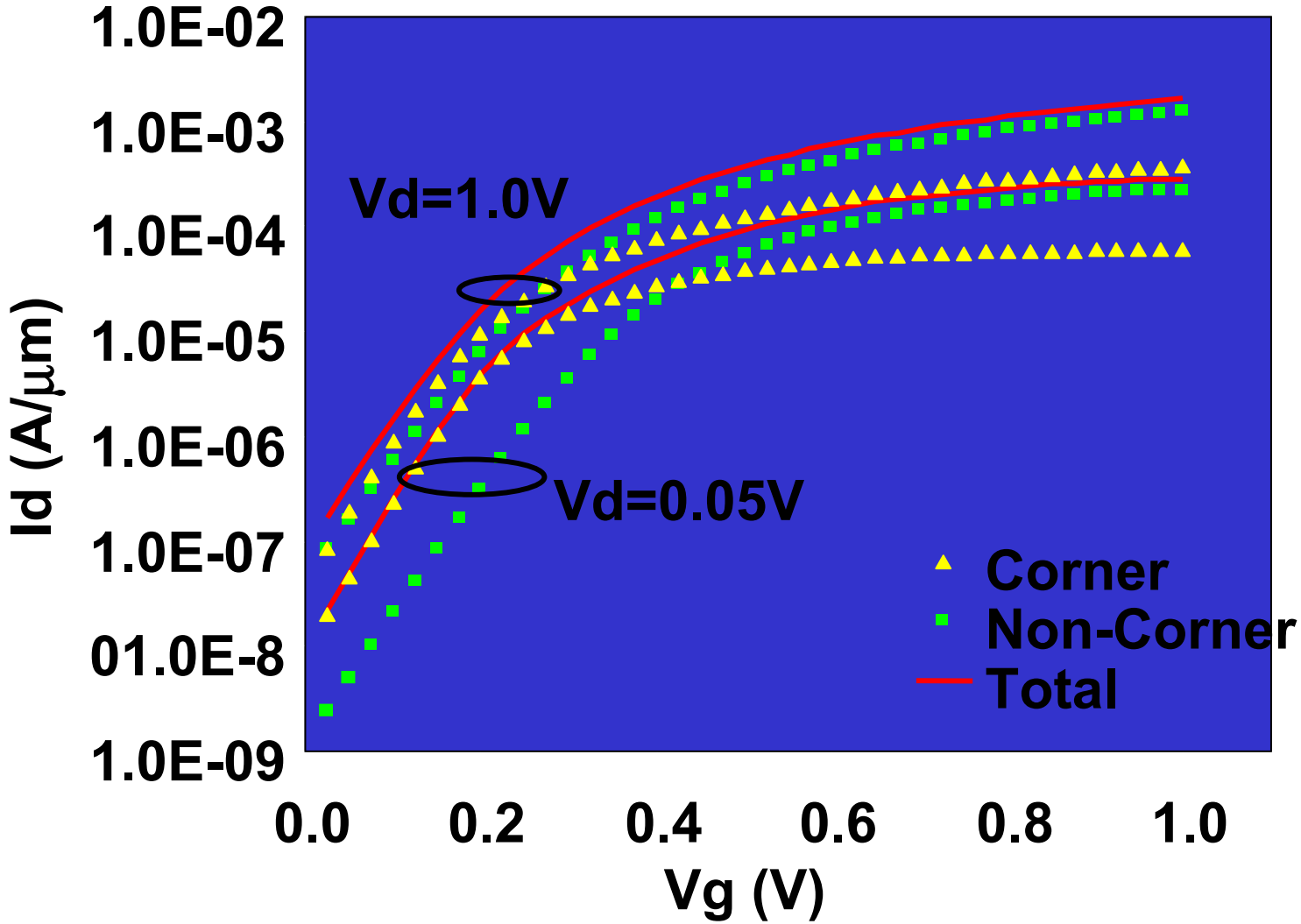
- **Excellent electrostatics and good device performance**

Tri-Gate Device Physics

- Three distinct regions of operation

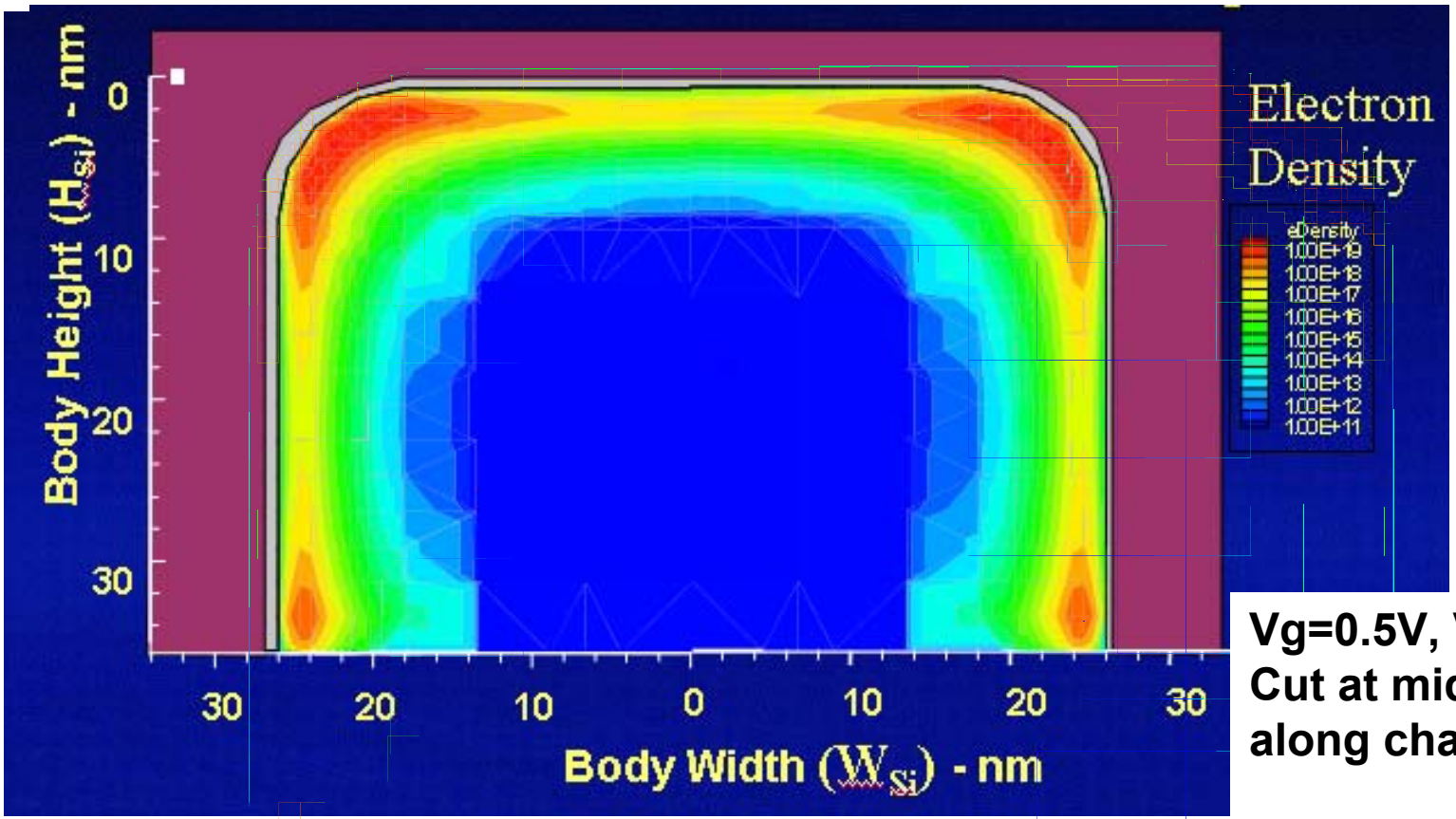


Components of Current in Tri-Gate



Corner device shows much improved ΔS & DIBL over non-corner devices because of proximity of adjacent gates

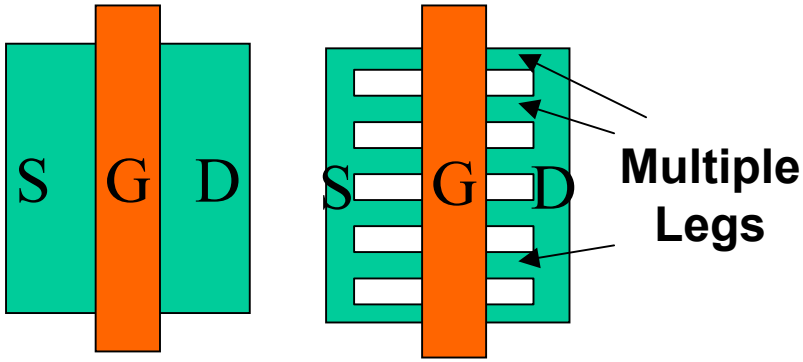
Physics of Corner Device

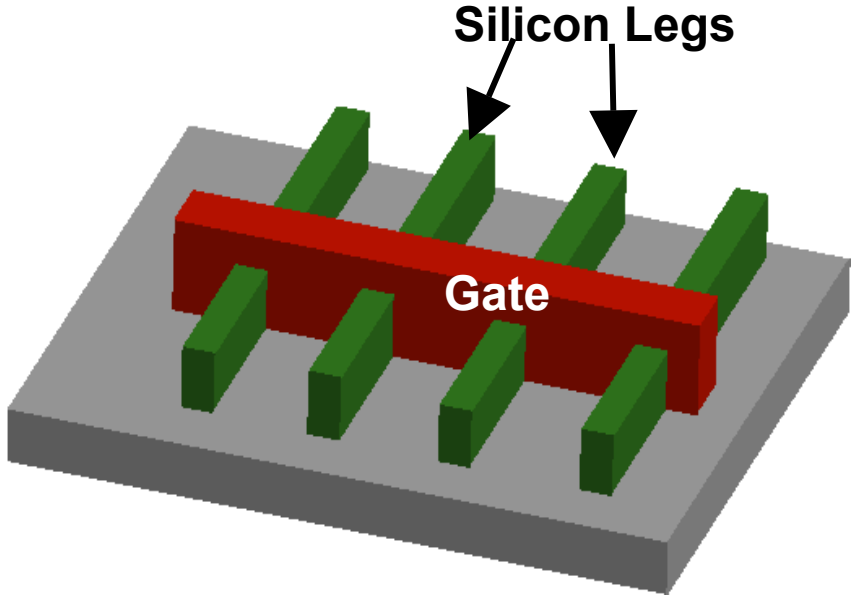


Vg=0.5V, Vd=1.0V
Cut at midpoint along channel

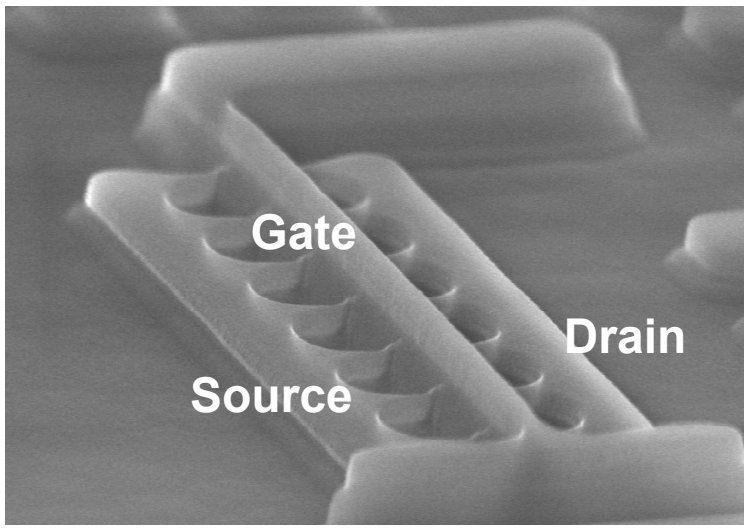
Proximity of the two gates at the corner give the nearly-ideal characteristics of the corner device, and the high current density

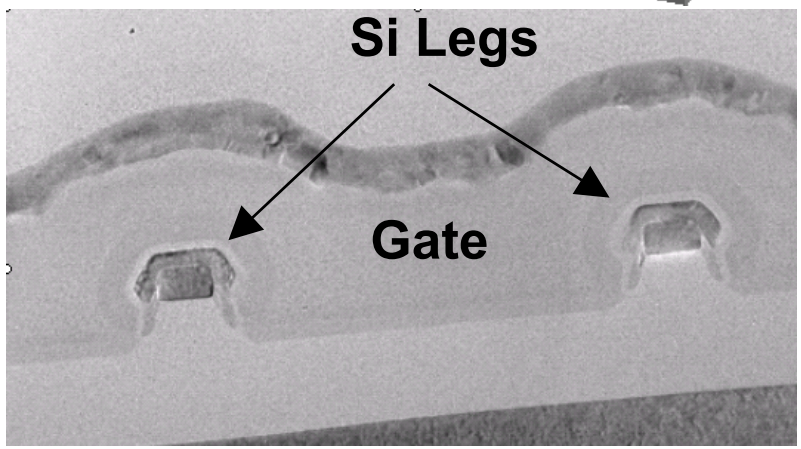
Tri-Gate Architecture





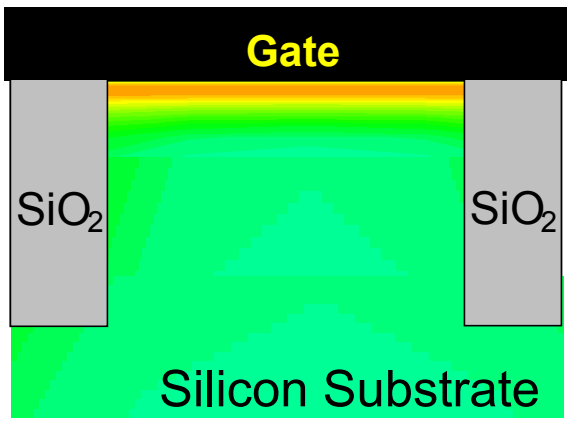
Total Drive Current =
I_d per Tri-gate Transistor x no. of Legs



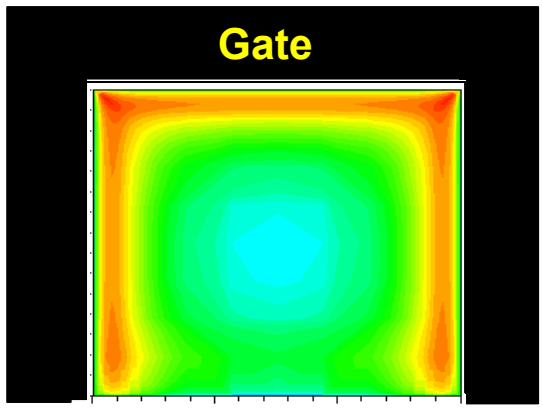


- **Tri-Gate architecture compatible with future devices such as nanowires and nanotubes**

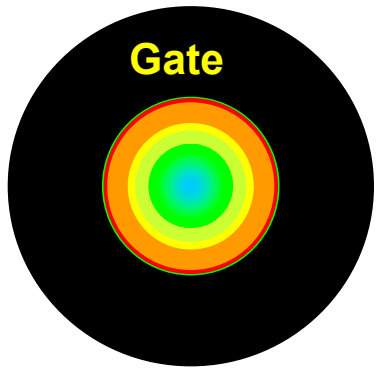
Nano-Device Structure Evolution



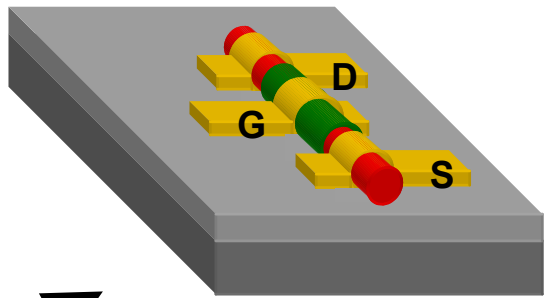
Planar Transistor

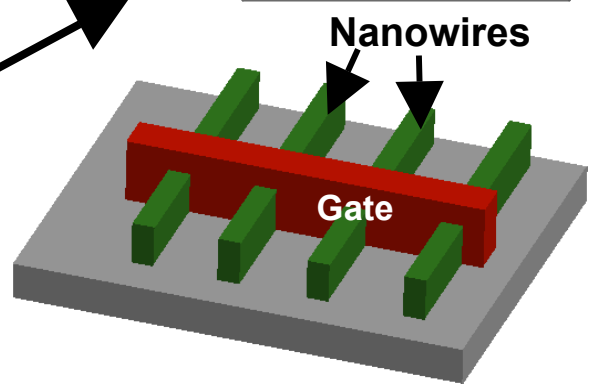


Non-Planar Tri-gate



Nanowire





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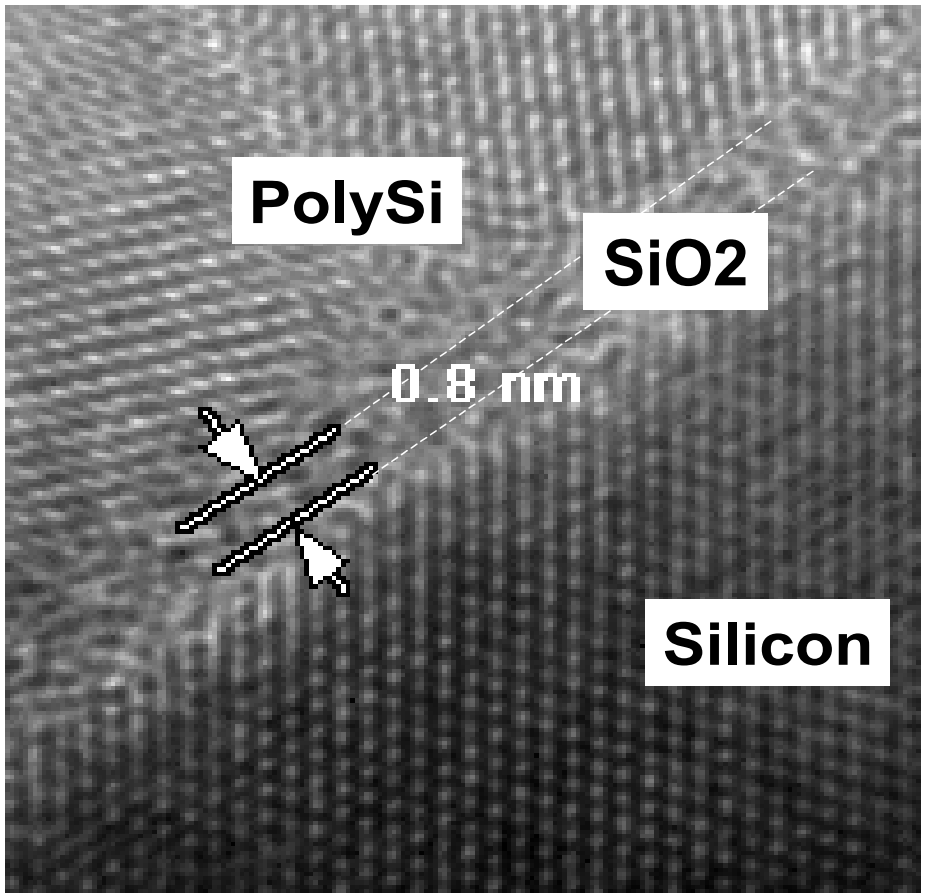
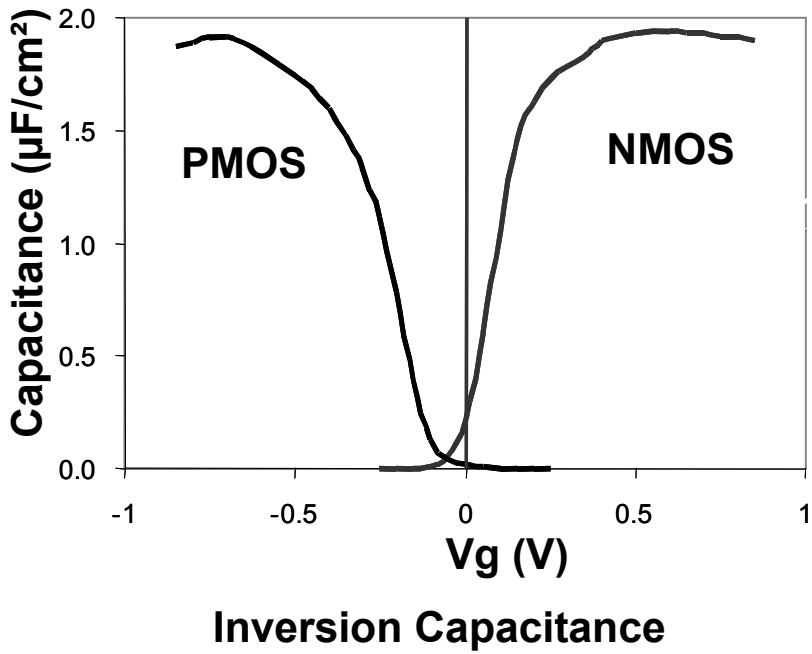
SiO2 Less Than 3 Atomic layers Thick

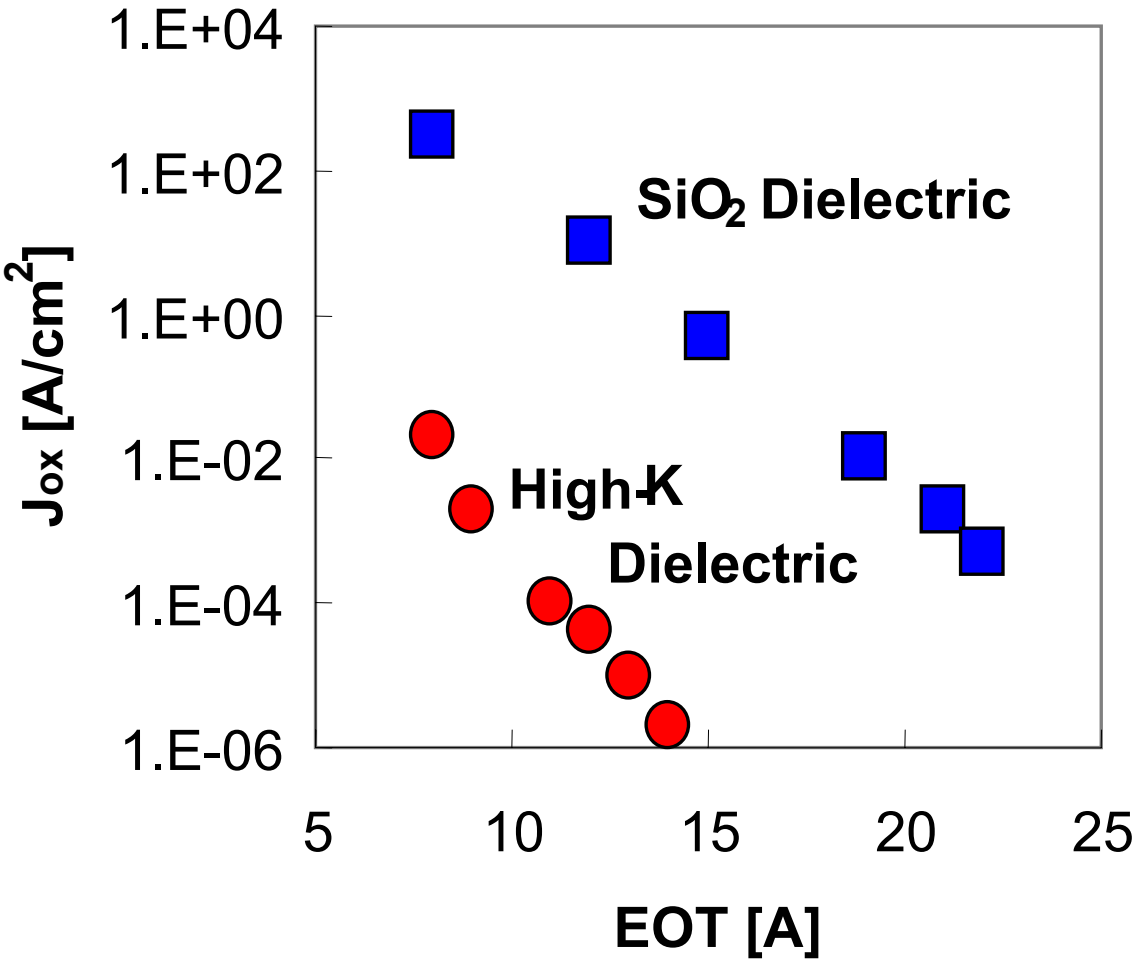




Inversion Capacitance

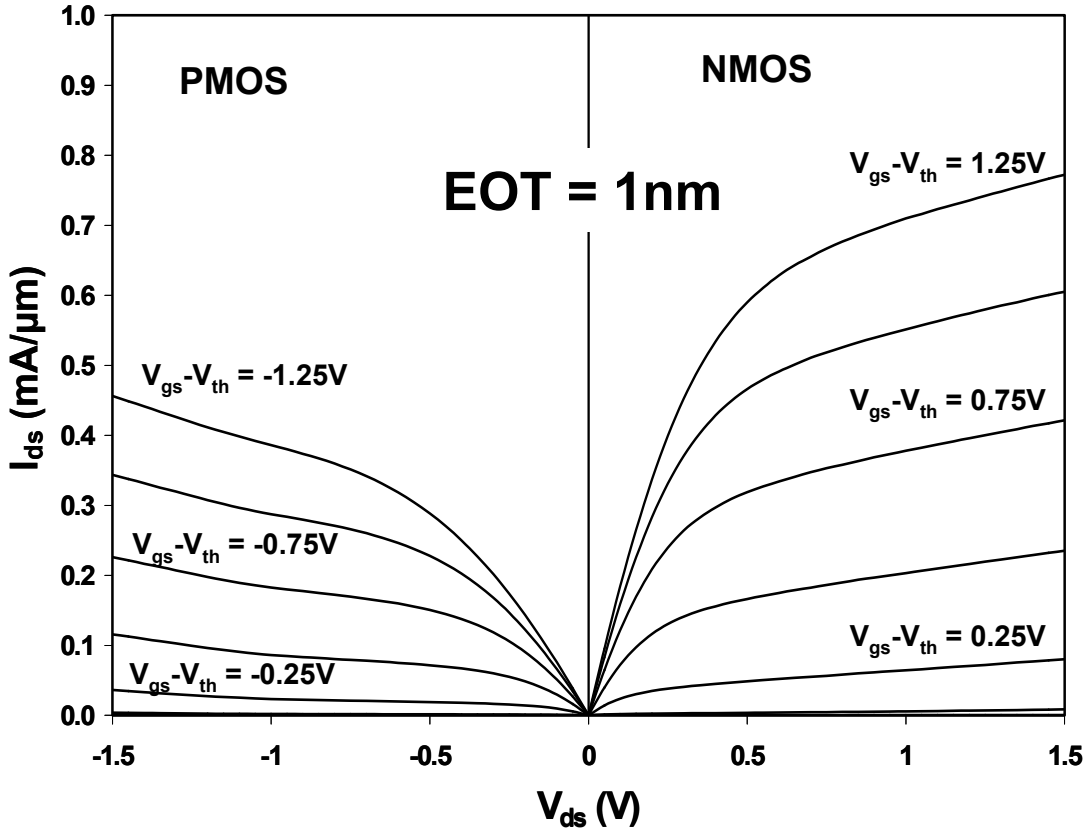
- SiO2 leakage is increasing with reducing thickness
- SiO2 gate oxide running out of atoms for further scaling

Alternative Gate Dielectric Required for Future-Generation Si Nano-Transistors



- **Higher gate capacitance, less gate leakage**

Si CMOS Transistor with Alternative Gate Dielectrics



- NMOS: Ft = 83GHz Fmax = 35GHz
- PMOS: Ft = 41GHz Fmax = 25GHz

Summary

- Research Si nano-transistors down to 10nm physical L_G have been demonstrated with improved intrinsic gate delay and energy-delay trends over devices with longer L_G
- Transistor off-state leakage increases with reducing physical L_G, and will need to be reduced for future logic products
  - 10nm research transistor exhibits degraded short channel performance and high off-state leakage
- Gate oxide leakage is increasing with reducing thickness and SiO2 is running out of atoms for further scaling
- The short-channel performance and off-state leakage of future Si nano-transistors will be improved using new transistor structure such as Tri-gate, and the gate oxide leakage will be reduced using alternative gate stacks